

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. DATUMTE.018A	APPLICATION NO. unknown <i>10820381</i>
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Plasterer, et al.	
(USE SEVERAL SHEETS IF NECESSARY)		FILING DATE Herewith	GROUP Unknown

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
AJ	6525571	2/25/03	Green			
	6501314	12/31/02	Ling			
	6424194	7/23/02	Hairapetian			
	6340899	1/22/02	Green			
	6320422	11/20/01	Koh			
	6028454	2/22/00	Elmasry et al.			
	6014041	1/11/00	Somasekhar et al.			
	5945858	8/31/99	Sato			
	5892382	4/6/99	Ueda et al.			
	5877642	3/2/99	Takahashi			
	5726613	3/10/98	Hayashi et al.			
	5216295	6/1/93	Hoang			
	5202655	7/13/93	Hara			
	4333020	6/1/82	Maerder			
↓	2003-0122603 A1	7/3/03	Green			

FOREIGN PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
						YES      NO

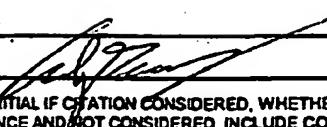
EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
AJ	Allam, M, et al., "Dynamic Current Mode Logic (DyCML): A New Low-Power High-Performance Logic Style," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 3, (March 2001), Institute of Electrical and Electronics Engineers, Inc., pp. 550-558.
	Hara, S., et al., "Broad-band Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifiers," <i>IEEE Transactions on Microwave Theory and Techniques</i> , Vol. MTT-36, No. 12, (Dec. 1998) Institute of Electrical and Electronics Engineers, Inc., pp. 1920-1924.
↓	Kiaei, S., et al., "CMOS Source-Coupled Logic for Mixed-Mode VLSI," <i>IEEE International Symposium on Circuits and Systems</i> (23rd: 1990: New Orleans), Institute of Electrical and Electronics Engineers, Inc., pp. 1608-1611. <i>no month</i>

EXAMINER <i>AJ</i>	DATE CONSIDERED <i>7/22/03</i>
*EXAMINER: INITIAL IF CITATION CONSIDERED. WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609, DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.	

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. DATUMTE.016A	APPLICATION NO. Unknown <i>1082038/</i>
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Plasterer, et al.	
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EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)		
AT	Kundan, J., et al., "Enhanced Folded Source-Coupled Logic Technique for Low-Voltage Mixed-Signal Integrated Circuits," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> , Vol. 47, No. 8 (Aug. 2000) Institute of Electrical and Electronics Engineers, Inc., pp. 810-817.		
	Tanabe, A., et al., "0.18-μm-CMOS 10-Gb/s Multiplexer/Demultiplexer ICs Using Current Mode Logic with Tolerance to Threshold Voltage Fluctuation," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 36, No. 6 (June 2001) Institute of Electrical and Electronics Engineers, Inc., pp. 988-996.		
JD	Yamashina, M., et al., "An MOS Current Mode Logic (MCML) Circuit For Low-Power Sub-Ghz Processors," <i>IEICE Transactions on Electronics</i> , Vol. E75-C (Oct. 1992), Institute of Electronics, Information and Communication Engineers, pp. 1181-1187.		

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EXAMINER	DATE CONSIDERED
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